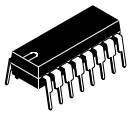


SLUS347A – MAY 1995 – REVISED APRIL 2003

9-LINE 3 TO 5 VOLT SCSI ACTIVE TERMINATOR, REVERSE DISCONNECT

FEATURES

- **Complies with SCSI, SCSI–2 and SPI–2 Standards**
- **2.7-V to 5.25-V Operation**
- **1.8-pF Channel Capacitance during Disconnect**
- **0.5-μA Supply Current in Disconnect Mode**
- **110-Ω/2.5-kΩ Programmable Termination**
- **Completely Meets SCSI Hot Plugging**
- **–400-mA Sourcing Current for Termination**
- **+400-mA Sinking Current for Active Negation Drivers**
- **Trimmed Termination Current to 4%**
- **Trimmed Impedance to 7%**
- **Current Limit and Thermal Shutdown Protection**

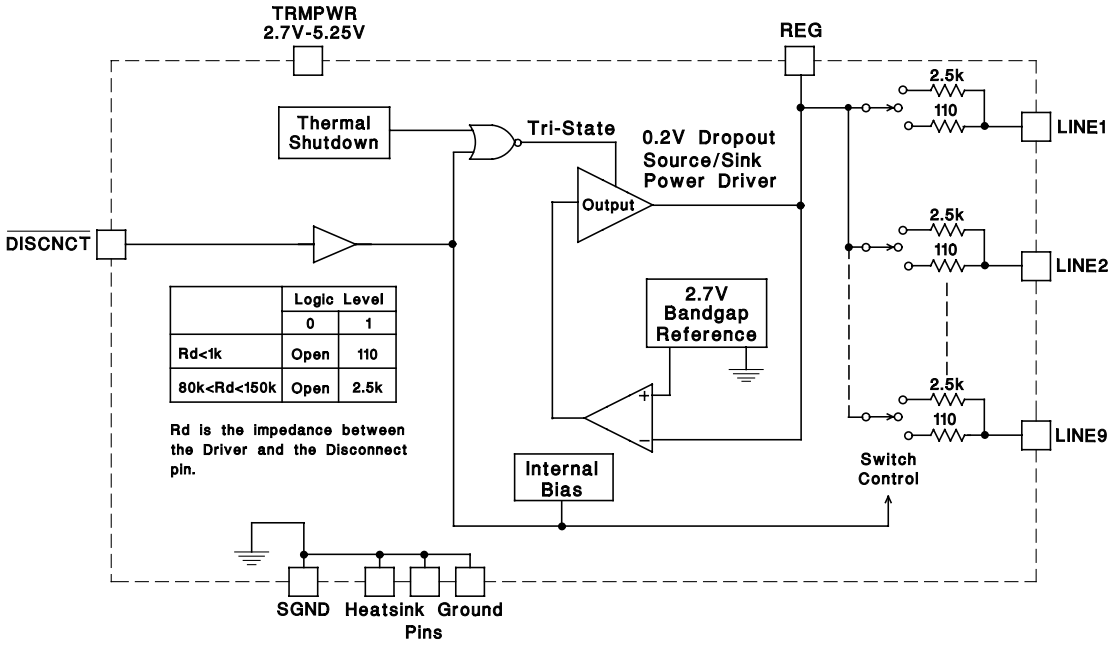
DESCRIPTION

The UCC5606 provides 9 lines of active termination for a small computer systems interface (SCSI) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UCC5606 is ideal for high performance 3.3-V SCSI systems. The key features contributing to such low operating voltage are the 0.1-V drop out regulator and the 2.7-V reference. During disconnect the supply current is typically only 0.5 μA, which makes the device attractive for battery powered systems.

The UCC5606 is designed with an ultra-low channel capacitance of 1.8 pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

BLOCK DIAGRAM



UDG–94067–1

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DESCRIPTION (CONTINUED)

The UCC5606 can be programmed for either a 110-Ω or 2.5-kΩ termination. The 110-Ω termination is used for standard SCSI bus lengths and the 2.5-kΩ termination is typically used in short bus applications. When driving the TTL compatible $\overline{\text{DISCNCT}}$ pin directly, the 110-Ω termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when low. When the $\overline{\text{DISCNCT}}$ pin is driven through an impedance between 80 kΩ and 150 kΩ, the 2.5-kΩ termination is connected when the $\overline{\text{DISCNCT}}$ pin is driven high, and disconnected when driven low.

The power amplifier output stage allows the UCC5606 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5606 is pin-for-pin compatible with Unitrode's other 9-line single-ended SCSI terminators, except that $\overline{\text{DISCNCT}}$ is now active low, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5606 is completely hot pluggable and appears as high impedance at the terminating channels with V_{TRMPWR} = 0 V or open.

Internal circuit trimming is utilized, first to trim the 110-Ω termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the maximum SCSI specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16-pin narrow body SOIC, 16-pin N and 24-pin TSSOP.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

	UCC5606	UNIT
TRMPWR voltage	7	V
Signal line voltage	0 to 7	
Regulator output current	0.6	A
Storage temperature, T_{stg}	–65 to 150	°C
Operating junction temperature, T_J	–55 to 150	
Lead temperature (soldering, 10 sec.)	300	

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
TRMPWR voltage	2.7		5.25	V
Signal line voltage	0		5	V
Disconnect input voltage	0		TRMPWR	°C

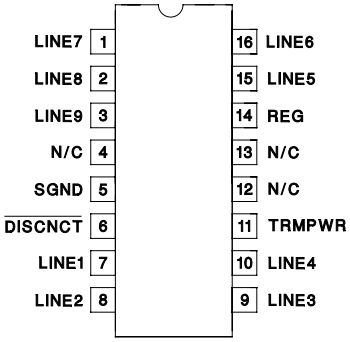
ORDERING INFORMATION

T_A	DISCONNECT STATUS	PACKAGED DEVICE†		
		DIL–16 (N)	SOIC–16 (DP)	TSSOP–24 (PWP)
0°C to 70°C		UCC5606N	UCC5606DP	UCC5606PWP

† The LQFP packages are available taped and reeled. Add TR suffix to device type (e.g. UCC5606PWPTR) to order quantities of 2,500 devices per reel.

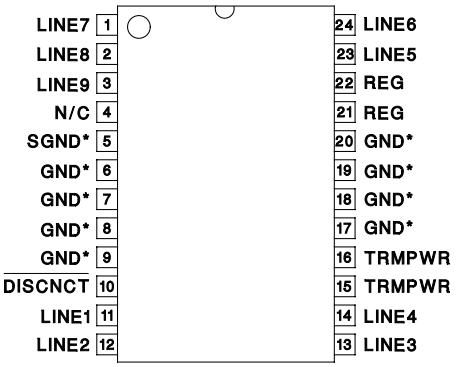
CONNECTION DIAGRAM

DIL–16 (Top View)
N Package



SOIC–16 (Top View)
DP Package

TSSOP–24 (Top View)
PWP Package



NOTE: GND* serves as a heat sink ground which must be tied to a large copper area or the grounding plate.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, $\overline{\text{DISCNCT}}$ = 3.3 V, $R_{DISCNCT}$ = 0 Ω, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr supply current	All termination lines = open		1	2	mA
	All termination lines = 0.2 V		210	218	
Power down mode	$\overline{\text{DISCNCT}}$ = 0 V		0.5	5.0	µA
Output Section (110 ohms – Terminator Lines)					
Terminator impedance		102.3	110.0	117.7	Ohms
Output high voltage	TRMPWR = 3 V (1)	2.5	2.7	3.0	V
Max output current	V_{LINE} = 0.2 V, T_J = 25°C	–22.1	–23.0	–24.0	mA
	V_{LINE} = 0.2 V	–21	–23	–24	
	V_{LINE} = 0.2 V, T_J = 25°C (1) TRMPWR = 3 V,	–20.2	–23.0	–24.0	
	V_{LINE} = 0.2 V, TRMPWR = 3 V (1)	–19	–23	–24	
	V_{LINE} = 0.5 V			–22.4	
Output leakage	$\overline{\text{DISCNCT}}$ = 0 V, TRMPWR = 0 V to 5.25 V		10	400	nA
Output capacitance	$\overline{\text{DISCNCT}}$ = 0 V, DP package (2)		1.8	2.5	pF
Output Section (2.5 kΩ – Terminator Lines) ($R_{DISCNCT}$ = 80 kΩ)					
Terminator impedance		2.0	2.5	3.0	kΩ
Output high voltage	TRMPWR = 3 V (1)	2.5	2.7	3.0	V
Max output current	V_{LINE} = 0.2 V	–0.7	–1.0	–1.4	mA
	V_{LINE} = 0.2 V, TRMPWR = 3 V (1)	–0.6	–1.0	–1.5	
Output leakage	$\overline{\text{DISCNCT}}$ = 0 V, TRMPWR = 0 to 5.25 V		10	400	nA
Output capacitance	$\overline{\text{DISCNCT}}$ = 0 V, DP package (2)		1.8	2.5	pF

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, $\overline{\text{DISCNCT}}$ = 3.3 V, $R_{DISCNCT}$ = 0 Ω, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section					
Regulator output voltage	5.25 V > TRMPWR > 3 V	2.5	2.7	3.0	V
Drop-out voltage	All termination lines = 0.2 V		0.1	0.2	
Short circuit current	V_{REG} = 0 V	–200	–400	–800	mA
Sinking current capability	V_{REG} = 3 V	200	400	800	
Thermal shutdown	(2)		170		°C
Thermal shutdown hysteresis	(2)		10		
Disconnect Section					
Disconnect threshold	$R_{DISCNCT}$ = 0 kΩ to 80 kΩ	0.8	1.5	2.0	V
Input current	$\overline{\text{DISCNCT}}$ = 3.3 V		30	50	µA

NOTES: 1. Measuring each termination line while other eight are low (0.2 V).
2. Ensured by design. Not production tested.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{DISCNCT}}$	7	I	Taking this pin low causes the 9 channels to become high impedance and the chip to go into low power mode. In short laptop buses an 80-kΩ to 150-kΩ resister to TERPWR terminates the bus at 2.5 kΩ. Less than 110 Ω to TERPWR enables the terminator.
GND	9		Ground reference for the device
LINE1 TO LINE9	4	I	110-Ω termination channels
REG	9	I	Output of the internal 2.7-V regulator
TRMPWR	4		Power for the device
GND*			Heat sink ground, must be tied to a large copper area or the grounding plate.

APPLICATION INFORMATION

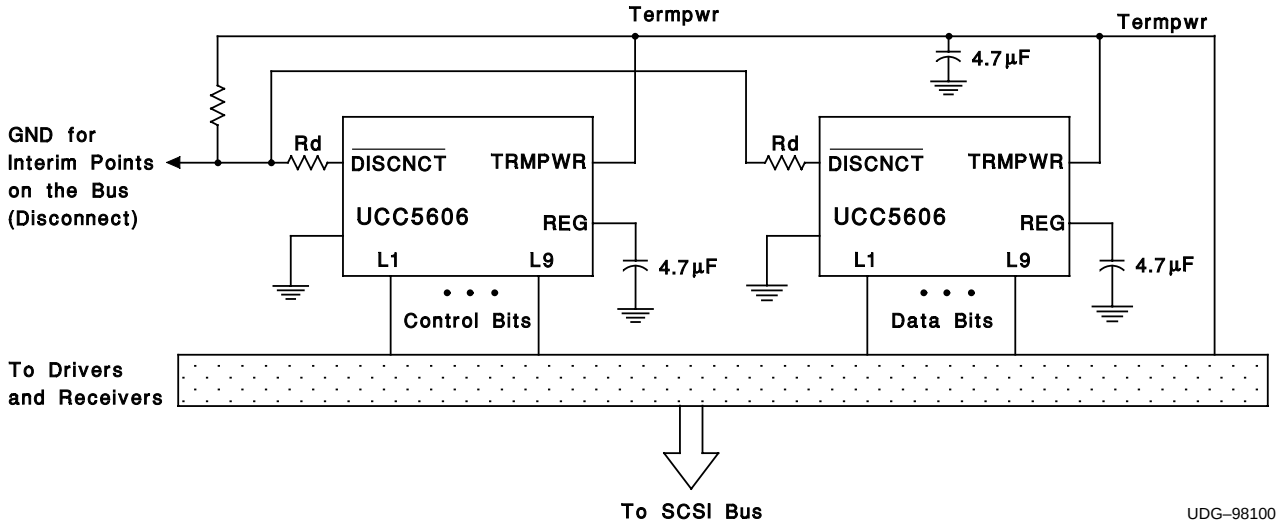


Figure 1. Typical SCSI Bus Configurations Utilizing two UCC5606 Devices

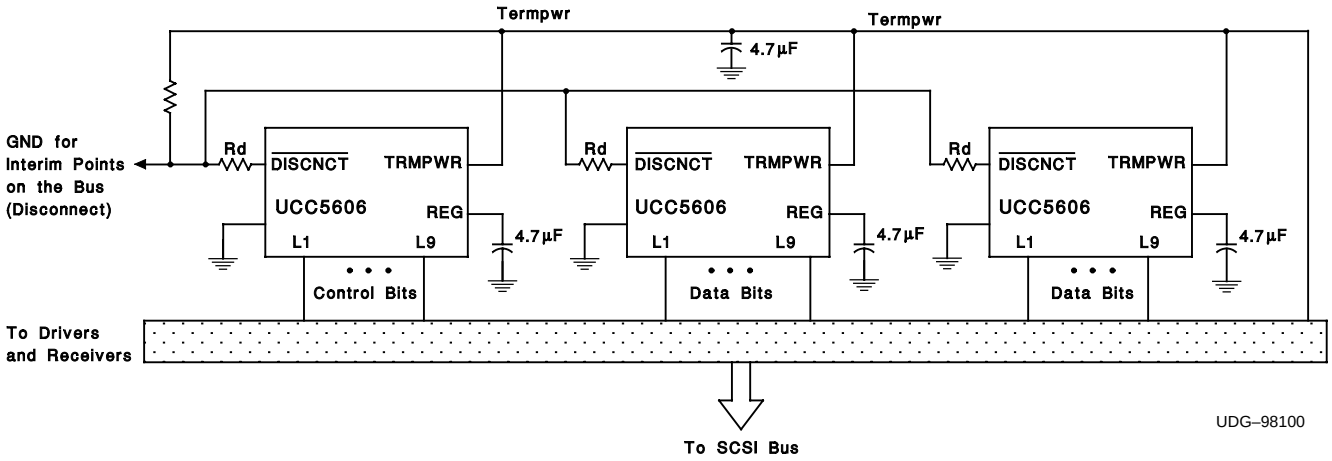


Figure 2. Typical Wide SCSI Bus Configurations Utilizing three UCC5606 Devices

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5606PWPTR	LIFEBUY	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC5606PWP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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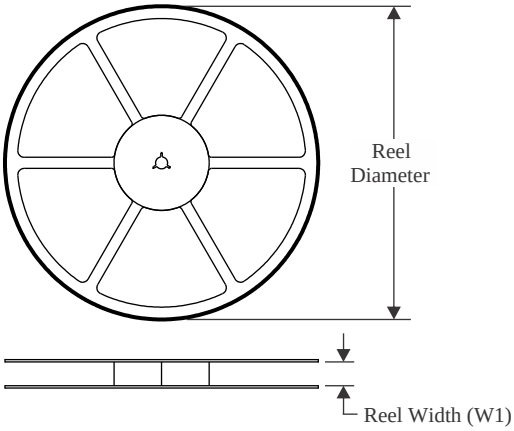
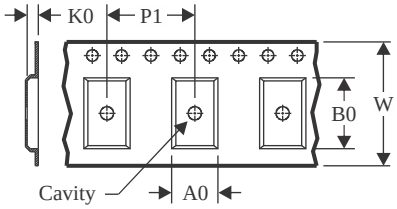
TAPE AND REEL INFORMATION

REEL DIMENSIONS

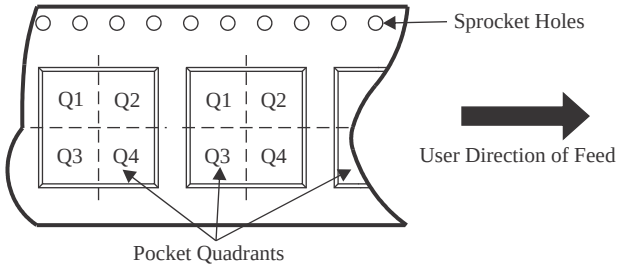


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

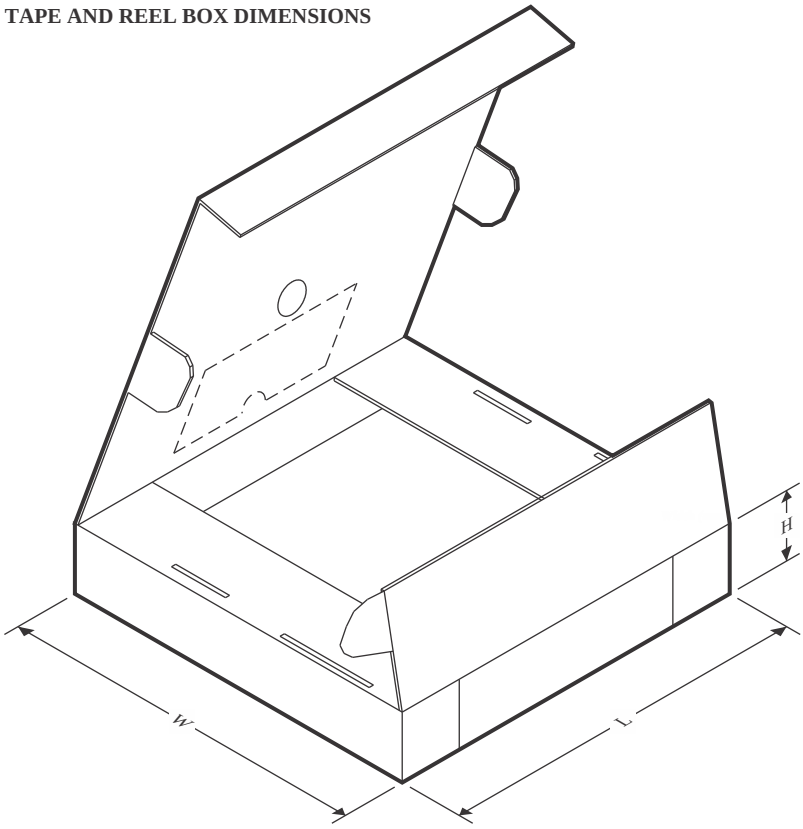
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5606PWPTR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

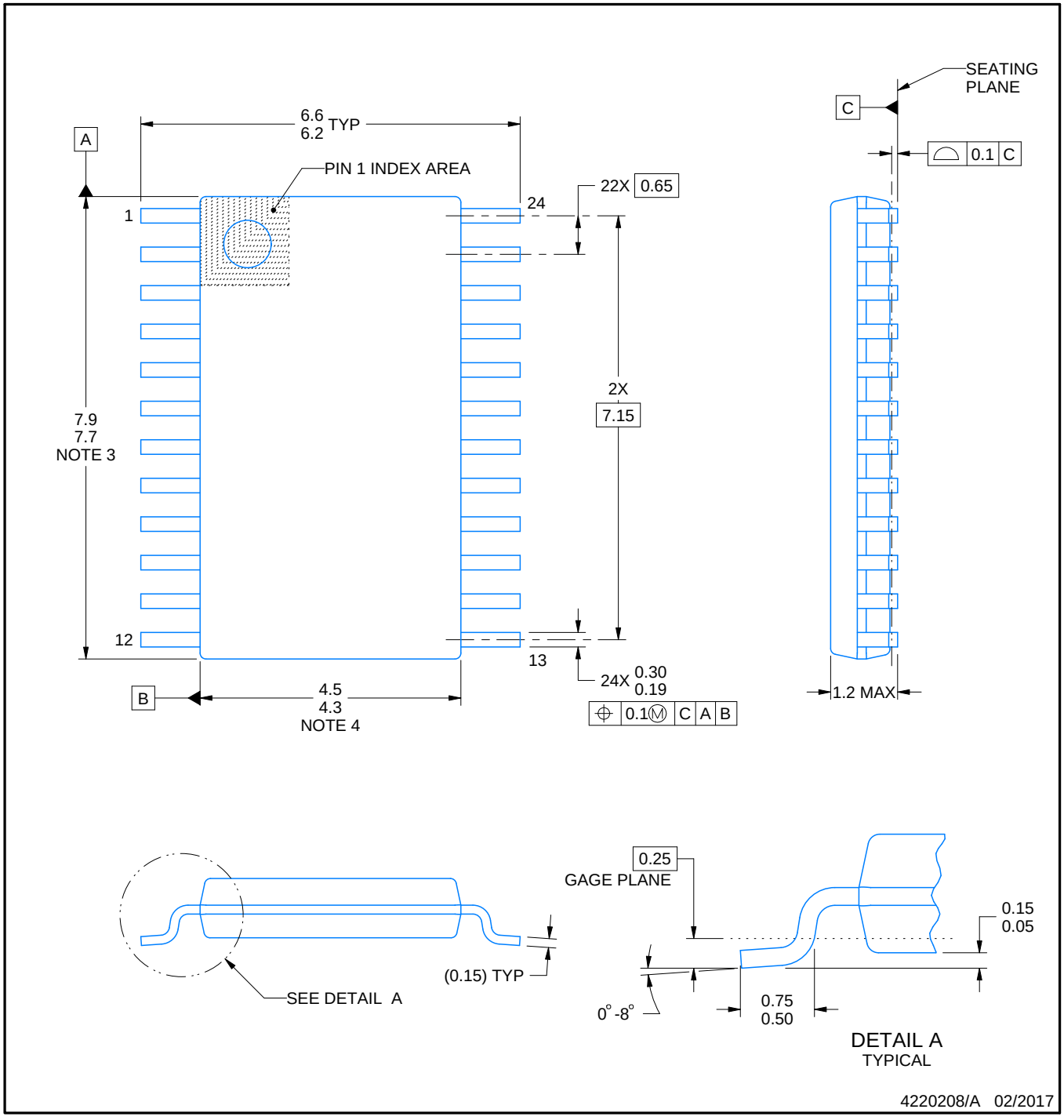
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5606PWPTR	TSSOP	PW	24	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0024A

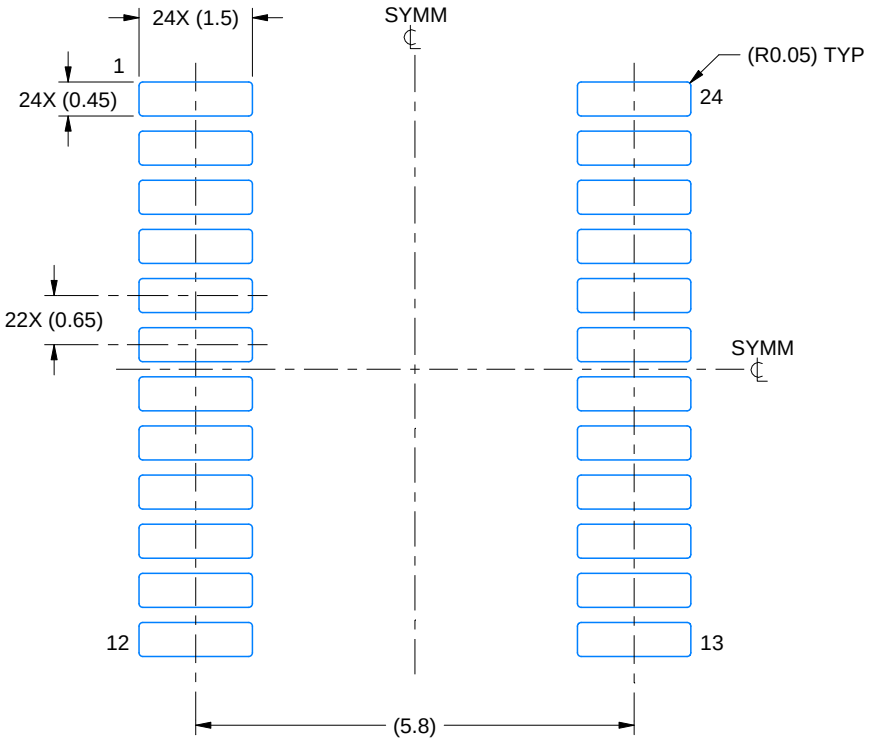
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

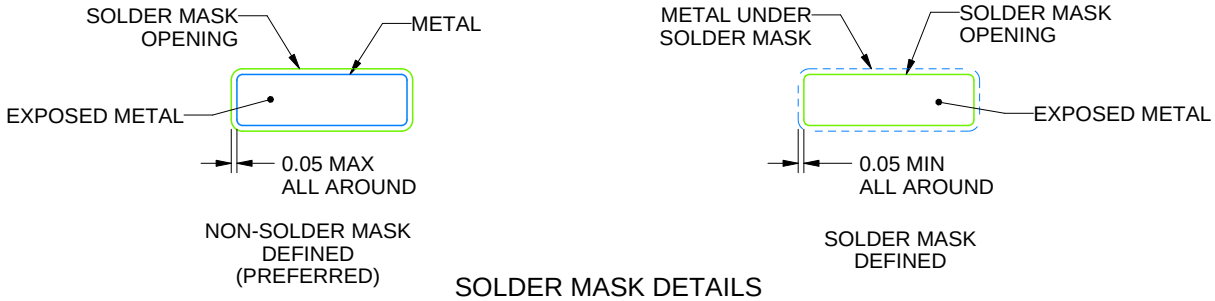


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

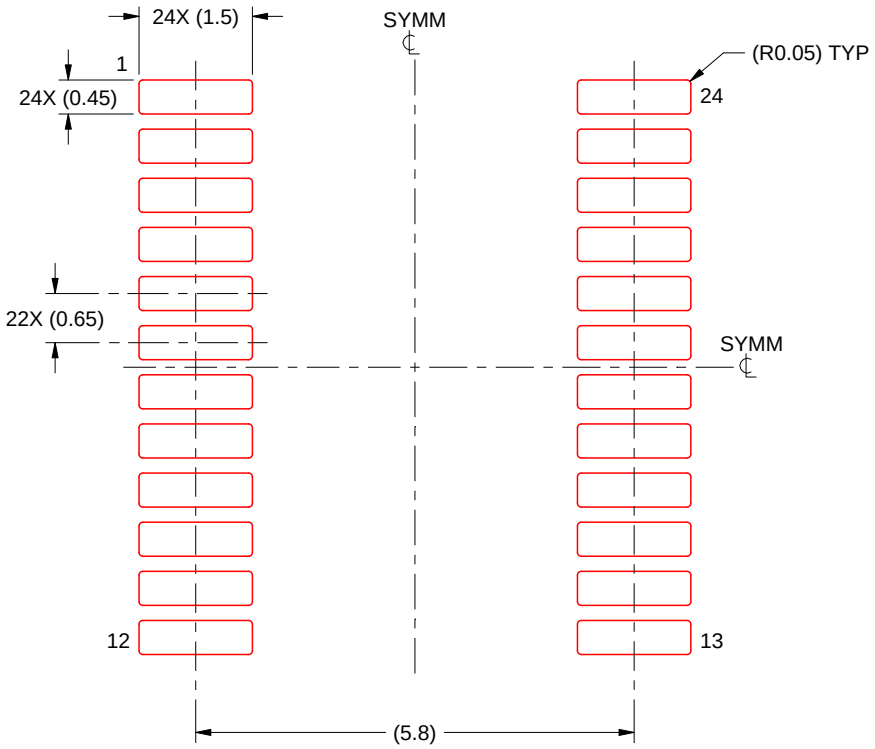


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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